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LERNER AND GREENBERG, P.A.
PATENT ATTORNEYS AND ATTORNEYS AT LAW
2445 Hollywood Boulevard
Hollywood, Florida 33020
Tel: (954) 925-1100
Fax: (954) 925-1101

PATENTUSA[SM]
www.patentusa.com
patents@patentusa.com

Mailing Address:
Post Office Box 2480
Hollywood, FL 33022-2480

New York Office
153 E 57th Street
Suite 15G
New York, NY 10022

Herbert L. Lerner (NY Bar)
Laurence A. Greenberg (FL Bar)

Werner H. Stemer (FL Bar), Senior Attorney

Ralph E. Locher (FL, IL, MO Bars)
Manfred Beck (US & German Pat. Agent)
Mark P. Weichselbaum (TN Bar)
Gregory L. Mayback (FL Bar)
Markus Nolff (FL Bar)
Otto S. Kauder (Reg. Pat. Agent)
Loren Donald Pearson (FL Bar)

"Express Mail" mailing label number EL608557604US
Date of Deposit October 10, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Michael Burns
MICHAEL BURNS

Docket No.: GR 98 P 1507

Date: October 10, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : ANDREAS RUSCH ET AL.

Title : SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING IT

2 sheets of formal drawings in triplicate.
A check in the amount of $ 710.00 covering the filing fee.
PCT Publication (cover sheet only).

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicants

WERNER H. STEMER
REG. NO. 34,956

LAG:kc

WELTORGANISATION FÜR GEISTIGES EIGENTUM
Internationales Büro

PCT

INTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

(51) Internationale Patentklassifikation 6: H01L 27/112, 21/8246 — A1

(11) Internationale Veröffentlichungsnummer: WO 99/53546

(43) Internationales Veröffentlichungsdatum: 21. Oktober 1999 (21.10.99)

(21) Internationales Aktenzeichen: PCT/DE99/00901

(22) Internationales Anmeldedatum: 25. März 1999 (25.03.99)

(30) Prioritätsdaten:
198 15 874.2 8. April 1998 (08.04.98) DE

(71) Anmelder (*für alle Bestimmungsstaaten ausser US*): SIEMENS AKTIENGESELLSCHAFT [DE/DE]; Wittelsbacherplatz 2, D-80333 München (DE).

(72) Erfinder; und
(75) Erfinder/Anmelder (*nur für US*): RUSCH, Andreas [DE/DE]; Sebnitzer Strasse 55, D-01099 Dresden (DE). ROTHENHÄUSSER, Steffen [DE/DE]; Louisenstrasse 5, D-01099 Dresden (DE). TRÜBY, Alexander [DE/DE]; Kamenzer Strasse 13 B, D-01099 Dresden (DE). OTANI, Yoichi [JP/DE]; Königsbrücker Strasse 109, D-01478 Weixdorf (DE). ZIMMERMANN, Ulrich [DE/US]; Appleblossom Drive, Mechanicsville, VA 23116 (US).

(74) Gemeinsamer Vertreter: SIEMENS AKTIENGESELLSCHAFT; Wittelsbacherplatz 2, D-80333 München (DE).

(81) Bestimmungsstaaten: JP, KR, US, europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Veröffentlicht
Mit internationalem Recherchenbericht.
Vor Ablauf der für Änderungen der Ansprüche zugelassenen Frist; Veröffentlichung wird wiederholt falls Änderungen eintreffen.

(54) Title: SEMICONDUCTOR MEMORY AND METHOD FOR PRODUCING SAME

(54) Bezeichnung: HALBLEITER-SPEICHERVORRICHTUNG UND VERFAHREN ZU DEREN HERSTELLUNG

(57) Abstract

The invention relates to a semiconductor memory with a matrix of semiconductor memory elements arranged in a substrate (10), which each comprise: a substrate area (10) of a first conductivity type; an insulating layer area (20) provided for on the substrate area (10); a via hole area (25) provided for in the insulating layer area (20); a bit fixing area (30) provided for in the substrate area (10) below the via hole area (25); and a contact pin area (40) which is provided for in the via hole area (25) and is in electric contact with the bit fixing area (30). The bit fixing area (30) is configured in such a way that it fixes the contact resistance between the substrate area (10) and the contact pin area (40) in accordance with the bit to be fixed in each semiconductor memory element.